National Semiconductor

LP38853
3A Fast-Response High-Accuracy Adjustable LDO Linear Regulator with Enable and Soft-Start

General Description

The LP38853-ADJ is a high current, fast response regulator which can maintain output voltage regulation with extremely low input to output voltage drop. Fabricated on a CMOS process, the device operates from two input voltages: V_{BIAS} provides voltage to drive the gate of the N-MOS power transistor, while V_{IN} is the input voltage which supplies power to the load. The use of an external bias rail allows the part to operate from ultra low V_{IN} voltages. Unlike bipolar regulators, the CMOS architecture consumes extremely low quiescent current at any output load current. The use of an N-MOS power transistor results in wide bandwidth, yet minimum external capacitance is required to maintain loop stability.

The fast transient response of this device makes it suitable for use in powering DSP, Microcontroller Core voltages and Switch Mode Power Supply post regulators. The part is available in PSOP 8–pin, TO-220 7–pin, and TO-263 7-pin packages.

Dropout Voltage: 240 mV (typical) at 3A load current.

Low Ground Pin Current: 10 mA (typical) at 3A load current.

Soft-Start: Programmable Soft-Start time.

Precision ADJ Voltage: ±1.5% for T_J = 25°C, and ±2.0% for 0°C ≤ T_J ≤ +125°C, across all line and load conditions

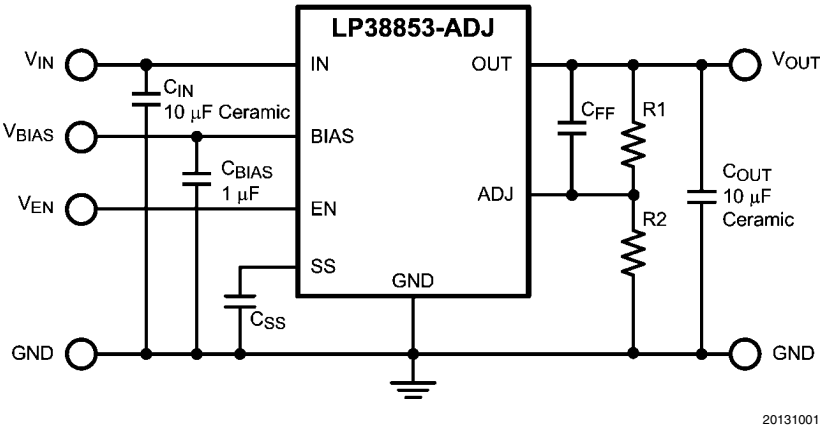
Features

- Adjustable V_{OUT} range of 0.80V to 1.8V
- Wide V_{BIAS} Supply operating range of 3.0V to 5.5V
- Stable with 10µF Ceramic capacitors
- Dropout voltage of 240 mV (typical) at 3A load current
- Precision V_{ADJ} across all line and load conditions:
  - — ±1.5% V_{ADJ} for T_J = 25°C
  - — ±2.0% V_{ADJ} for 0°C ≤ T_J ≤ +125°C
  - — ±3.0% V_{ADJ} for -40°C ≤ T_J ≤ +125°C
- Over-Temperature and Over-Current protection
- Available in 8 lead PSOP, 7 lead TO-220 and 7 lead TO-263 packages
- –40°C to +125°C Operating Junction Temperature Range

Applications

- ASIC Power Supplies in:
  - Desktops, Notebooks, and Graphics Cards, Servers
  - Gaming Set Top Boxes, Printers and Copiers
- Server Core and I/O Supplies
- DSP and FPGA Power Supplies
- SMPS Post-Regulator

Typical Application Circuit



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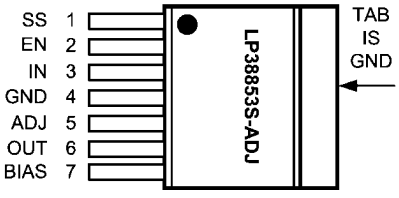
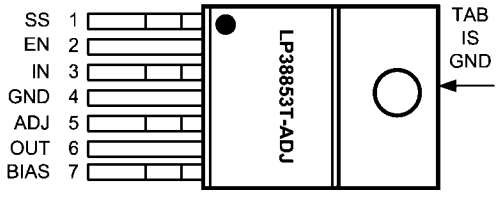
Ordering Information

V_{OUT}	Order Number	Package Type	Package Drawing	Supplied As
ADJ	LP38853S-ADJ	TO263-7	TS7B	Rail of 45
	LP38853SX-ADJ	TO263-7	TS7B	Tape and Reel of 500
	LP38853T-ADJ	TO220-7	TA07B	Rail of 45
	LP38853MR-ADJ	PSOP-8	MR08B	Rail of 95
	LP38853MRX-ADJ	PSOP-8	MR08B	Tape and Reel of 2500

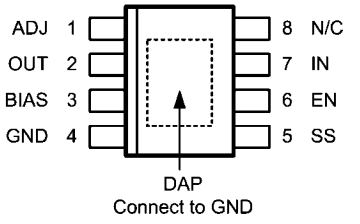
Connection Diagrams



TO263-7, Top View



TO220-7, Top View



PSOP-8, Top View

Pin Descriptions

TO220-7 Pin #	TO263-7 Pin #	PSOP-8 Pin #	Pin Symbol	Pin Description
1	1	5	SS	Soft-Start capacitor connection. Used to control the rise time of V_{OUT} at turn-on.
2	2	6	EN	Device Enable, High = On, Low = Off.
3	3	7	IN	The unregulated voltage input
4	4	4	GND	Ground
5	5	1	ADJ	The feedback connection to set the output voltage
6	6	2	OUT	The regulated output voltage
7	7	3	BIAS	The supply for the internal control and reference circuitry.
-	-	8	N/C	No internal connection
TAB	TAB	-	TAB	The TO220 and TO263 TAB is a thermal and electrical connection that is physically attached to the backside of the die, and used as a thermal heat-sink connection. See the Application Information section for details.
-	-	DAP	DAP	The PSOP DAP is a thermal connection only that is physically attached to the backside of the die, and used as a thermal heat-sink connection. See the Application Information section for details.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature Range	−65°C to +150°C
Lead Temperature	
Soldering, 5 seconds	260°C
ESD Rating	
Human Body Model (Note 2)	±2 kV
Power Dissipation (Note 3)	Internally Limited
V_{IN} Supply Voltage (Survival)	−0.3V to +6.0V
V_{BIAS} Supply Voltage (Survival)	−0.3V to +6.0V
V_{SS} SoftStart Voltage (Survival)	−0.3V to +6.0V
V_{OUT} Voltage (Survival)	−0.3V to +6.0V
I_{OUT} Current (Survival)	Internally Limited
Junction Temperature	−40°C to +150°C

Operating Ratings (Note 1)

V_{IN} Supply Voltage	$(V_{OUT} + V_{DO})$ to V_{BIAS}
V_{BIAS} Supply Voltage	
$0.8V \le V_{OUT} \le 1.2V$	3.0V to 5.5V
$1.2V < V_{OUT} \le 1.8V$	4.5V to 5.5V
V_{EN} Voltage	0.0V to V_{BIAS}
I_{OUT}	0 mA to 3.0A
Junction Temperature Range (Note 3)	−40°C to +125°C

Electrical Characteristics

Unless otherwise specified: V_{OUT} = 0.80V, $V_{IN} = V_{OUT(NOM)}$ + 1V, V_{BIAS} = 3.0V, $V_{EN} = V_{BIAS}$, I_{OUT} = 10 mA, $C_{IN} = C_{OUT}$ = 10 µF, C_{BIAS} = 1 µF, C_{SS} = open. Limits in standard type are for T_J = 25°C only; limits in **boldface type** apply over the junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{ADJ}	V_{ADJ} Accuracy	$V_{OUT(NOM)}+1V \le V_{IN} \le V_{BIAS} \le 4.5V$, See (Note 7) $3.0V \le V_{BIAS} \le 5.5V$, $10\ mA \le I_{OUT} \le 3A$	492.5 **485.0**	500.	507.5 **515.0**	mV
		$V_{OUT(NOM)}+1V \le V_{IN} \le V_{BIAS} \le 4.5V$, See (Note 7) $3.0V \le V_{BIAS} \le 5.5V$, $10\ mA \le I_{OUT} \le 3.0A$, $0°C \le T_J \le +125°C$	490.0	500.	510.0	
V_{OUT}	V_{OUT} Range	$3.0V \le V_{BIAS} \le 5.5V$	0.80		1.20	V
		$4.5V \le V_{BIAS} \le 5.5V$	0.80		1.80	
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation, V_{IN} (Note 4)	$V_{OUT(NOM)}+1V \le V_{IN} \le V_{BIAS}$	-	0.04	-	%/V
$\Delta V_{OUT}/\Delta V_{BIAS}$	Line Regulation, V_{BIAS} (Note 4)	$3.0V \le V_{BIAS} \le 5.5V$	-	0.10	-	%/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Output Voltage Load Regulation (Note 5)	$10\ mA \le I_{OUT} \le 3.0A$	-	0.2	-	%/A
V_{DO}	Dropout Voltage (Note 6)	I_{OUT} = 3.0A	-	240	300 **450**	mV
$I_{GND(IN)}$	Quiescent Current Drawn from V_{IN} Supply	V_{OUT} = 0.80V V_{BIAS} = 3.0V $10\ mA \le I_{OUT} \le 3.0A$	-	7.0	8.5 **9.0**	mA
		$V_{EN} \le 0.5V$		1	10 **300**	µA
$I_{GND(BIAS)}$	Quiescent Current Drawn from V_{BIAS} Supply	$10\ mA \le I_{OUT} \le 3.0A$	-	3.0	3.8 **4.5**	mA
		$V_{EN} \le 0.5V$		100	170 **200**	µA
UVLO	Under-Voltage Lock-Out Threshold	V_{BIAS} rising until device is functional	2.20 **2.00**	2.45	2.70 **2.90**	V
$UVLO_{(HYS)}$	Under-Voltage Lock-Out Hysteresis	V_{BIAS} falling from UVLO threshold until device is non-functional	60 **50**	150	300 **350**	mV
I_{SC}	Output Short-Circuit Current	$V_{IN} = V_{OUT(NOM)}$ + 1V, V_{BIAS} = 3.0V, V_{OUT} = 0.0V	-	5.8	-	A

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Soft-Start						
r_{SS}	Soft-Start internal resistance		11.0	13.5	16.0	kΩ
t_{SS}	Soft-Start time $t_{SS} = C_{SS} \times r_{SS} \times 5$	C_{SS} = 10 nF	-	675	-	µs
Enable						
I_{EN}	ENABLE pin Current	$V_{EN} = V_{BIAS}$	-	0.01	-	µA
		V_{EN} = 0.0V, V_{BIAS} = 5.5V	-19 **-13**	-30	-40 **-51**	
$V_{EN(ON)}$	Enable Voltage Threshold	V_{EN} rising until Output = ON	1.00 **0.90**	1.25	1.50 **1.55**	V
$V_{EN(HYS)}$	Enable Voltage Hysteresis	V_{EN} falling from $V_{EN(ON)}$ until Output = OFF	50 **30**	100	150 **200**	mV
t_{OFF}	Turn-OFF Delay Time	R_{LOAD} x C_{OUT} << t_{OFF}	-	20	-	µs
t_{ON}	Turn-ON Delay Time	R_{LOAD} x C_{OUT} << t_{ON}	-	15	-	
AC Parameters						
PSRR (V_{IN})	Ripple Rejection for V_{IN} Input Voltage	$V_{IN} = V_{OUT(NOM)}$ + 1V, f = 120 Hz	-	80	-	dB
		$V_{IN} = V_{OUT(NOM)}$ + 1V, f = 1 kHz	-	70	-	
PSRR (V_{BIAS})	Ripple Rejection for V_{BIAS} Voltage	$V_{BIAS} = V_{OUT(NOM)}$ + 3V, f = 120 Hz	-	58	-	
		$V_{BIAS} = V_{OUT(NOM)}$ + 3V, f = 1 kHz	-	58	-	
e_n	Output Noise Density	f = 120 Hz	-	1	-	µV/√Hz
	Output Noise Voltage	BW = 10 Hz – 100 kHz	-	150	-	μV_{RMS}
		BW = 300 Hz – 300 kHz	-	90	-	
Thermal Parameters						
T_{SD}	Thermal Shutdown Junction Temperature		-	160	-	°C
$T_{SD(HYS)}$	Thermal Shutdown Hysteresis		-	10	-	
θ_{J-A}	Thermal Resistance, Junction to Ambient(Note 3)	TO220-7	-	60	-	°C/W
		TO263-7	-	60	-	
		PSOP-8	-	168	-	
θ_{J-C}	Thermal Resistance, Junction to Case(Note 3)	TO220-7	-	3	-	
		TO263-7	-	3	-	
		PSOP-8	-	11	-	

Note 1: Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but does not guarantee specific performance limits. For guaranteed specifications and conditions, see the Electrical Characteristics.

Note 2: The human body model is a 100 pF capacitor discharged through a 1.5k resistor into each pin. Test method is per JESD22-A114.

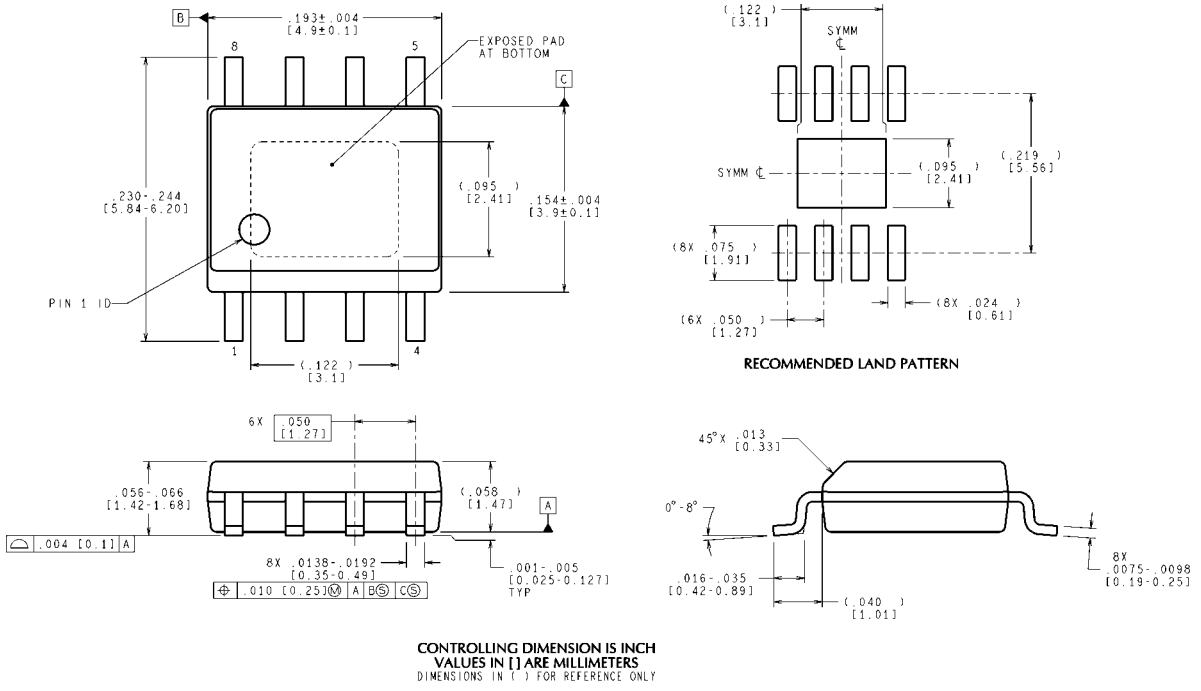
Note 3: Device power dissipation must be de-rated based on device power dissipation (P_D), ambient temperature (T_A), and package junction to ambient thermal resistance (θ_{JA}). Additional heat-sinking may be required to ensure that the device junction temperature (T_J) does not exceed the maximum operating rating. See the Application Information section for details.

Note 4: Output voltage line regulation is defined as the change in output voltage from nominal value resulting from a change in input voltage.

Note 5: Output voltage load regulation is defined as the change in output voltage from nominal value as the load current increases from no load to full load.

Note 6: Dropout voltage is defined as the input to output voltage differential (V_{IN} - V_{OUT}) where the input voltage is low enough to cause the output voltage to drop 2% from the nominal value.

Note 7: V_{IN} cannot exceed either V_{BIAS} or 4.5V, whichever value is lower.



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MRA08B (Rev B)

PSOP, 8 Lead, Molded, 0.050in Pitch
NS Package Number MRA08B